R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

SUPPORT FOR THE CLAIM AMENDMENTS

Support for the claim amendments may be found in the specification, for example, on page 5 lines 6-7, page 6 lines 3-4 and FIG. 4 as originally filed. Thus, no new matter has been added.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1-19 under 35 U.S.C. §102(e) as being anticipated by Swoboda et al. '929 (hereafter Swoboda) has been obviated in part by appropriate amendment, is respectfully traversed in part and should be withdrawn.

Swoboda concerns a dynamically configurable debug port for concurrent support of debug functions from multiple data processing cores (Title).

In contrast, claim 1 provides a boundary scan chain connected to each of said processors and said trace circuit. However, Swoboda appears to be silent regarding a boundary scan chain connected to each of the cores (asserted similar to the claimed processors) and a trace circuit as presently claimed. Claims 9 and 19 provide language similar to claim 1. As such, the

claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Regarding claims 2 and 10, the text of Swoboda cited on page 2 in the Office Action appears to be silent regarding a connector circuit configured to transfer data from a trace circuit **to a selected processor** as presently claimed. Therefore, the Examiner is respectfully requested to either (i) provide a clear and concise explanation how Swoboda allegedly anticipates the claim language or (ii) withdraw the rejection.

Regarding claims 3 and 11, the text of Swoboda cited on page 3 of the Office Action appears to be silent regarding transferring a first test data stream received by a selected processor **to a trace circuit** as presently claimed. Therefore, the Examiner is respectfully requested to either (i) provide a clear and concise explanation how Swoboda allegedly anticipates transferring a first test data stream to a trace circuit or (ii) withdraw the rejection.

Regarding claims 4 and 12, the text of Swoboda cited on page 3 of the Office Action appears to be silent regarding transferring a second test data stream received by a selected processor to a trace circuit as presently claimed. Therefore, the Examiner is respectfully requested to either (i) provide a clear and concise explanation how Swoboda allegedly anticipates

transferring a second test data stream to a trace circuit or (ii) withdraw the rejection.

Regarding claim 5, the Office Action has failed to establish that Swoboda discloses a first circuit and a second circuit as presently claimed. Therefore, *prima facie* anticipation has not been established. The Examiner is respectfully requested to either (i) provide specific evidence where Swoboda allegedly teaches all of the claim 5 limitations or (ii) withdraw the rejection.

Regarding claims 6 and 7, despite the assertion on page 3 of the Office Action, the cited text of Swoboda appears to be silent regarding a first and a second plurality of gates each coupled to one of the processors as presently claimed. Therefore, the Examiner is respectfully requested to either (i) clearly identify where Swoboda allegedly teaches the gates of claims 6 and 7 or (ii) withdraw the rejections.

Regarding claim 8, Swoboda appears to be silent regarding logical AND gates having at least one input configured to receive a select signal as presently claimed. As such, claim 8 is fully patentable over the cited reference and the rejection should be withdrawn.

Regarding claims 13 and 14, the text of Swoboda cited on page 5 of the Office Action appears to be silent regarding a step for presenting two predetermined logic states to the processors

other than a selected processor as presently claimed. Therefore, the Examiner is respectfully requested to either (i) clearly identify where Swoboda allegedly discloses the presenting steps of claim 13 and 14 or (ii) withdraw the rejection.

Regarding claims 16 and 18, despite the assertion on page 5 of the Office Action, the cited text of Swoboda appears to be silent regarding gating data and gating a test data stream in response to a select signal as presently claimed. As such, claims 16 and 18 fully patentable over the cited reference and the rejection should be withdrawn.

The Examiner is respectfully requested to refrain from omnibus rejections that simply list all of the claimed elements and then assert that the claimed elements are disclosed somewhere among the same two columns of text (see MPEP 707.07(d)).

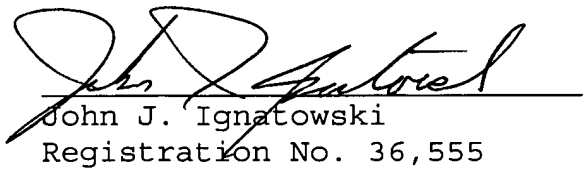
Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative at 586-498-0670 should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge Deposit Account No. 12-2252.

Respectfully submitted,

CHRISTOPHER P. MAIORANA, P.C.



John J. Ignatowski
Registration No. 36,555

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c/o Sandeep Jaggi
LSI Logic Corporation
1621 Barber Lane, M/S D-106 Legal
Milpitas, CA 95035

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